NEW SCHEME

CS33

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality in Boolean algebra. Write the duals of the following Boolean theorems:

i) $a + b + ab = a + b$

ii) $a + b + \overline{a}\,\overline{b} = 1$

iii) $ab + bc + \overline{c}a = bc + \overline{c}a$ (8 Marks)

(b) Complement the following Boolean expressions and write them as the sum of minterms.

i) $\overline{a} + \overline{b} + \overline{c} + \overline{d}$

ii) $ab + \overline{(abcd)}$ (6 Marks)

(c) Rewrite the following Boolean expressions in the M-notation and simplify :

i) $(a + b)(a + c)$

ii) $(a + b)(b + c)(\overline{c} + a)$ (6 Marks)

2. (a) What ia a universal gate? Consider a gate which takes two inputs A and B and produces an output $\overline{A} \cdot B$. Would you consider it a universal gate? Discuss. (10 Marks)

(b) Get the minimised sum-of products expression for

$f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 8, 9)$

with don't cares : $\sum m(10, 11, 12, 13, 14, 15)$

Use Karnaugh map for simplification. (10 Marks)

3. (a) Give the truth table for a binary full adder function and obtain the irredundant disjunctive normal expression for the function. Show how the function could be realised using NAND gates. (10 Marks)

(b) Use Quine McCluskey method and simplify the following function : $f(a, b, c, d) = \sum m(0, 1, 2, 3, 8, 9)$ (10 Marks)

4. (a) Explain the following properties of integrated circuits of the SSI type (small scale integration type)

i) Propagation delay

ii) Noise margin

iii) Fan - in

iv) Fan-out

Compare TTL and CMOS gates, in respect of these properties. (10 Marks)

(b) With a circuit diagram, explain the operation of the CMOS NAND gate. What are its advantages over corresponding TTL gates? (10 Marks)

Contd.... 2

5. (a) Explain clearly the Totem pole output stage and the Three-state output stage of a TTL gate. When would the three state stage be useful? **(10 Marks)**

   (b) What is a look-ahead carry adder? Explain the circuit and operation of a 4-bit binary adder with look-ahead carry. **(10 Marks)**

6. (a) How would you realise the function

   $ABCD + \overline{A}BC + B\overline{C}\,\overline{D}$ using an 8-to -1 multiplexer? **(10 Marks)**

   2v (b) Distinguish between PLA and PAL. Show how you would realise a Boolean function using a PLA. **(10 Marks)**

7. (a) Explain the operation of a simple SR flip flop using NAND gates. **(10 Marks)**

   (b) Draw the circuit and explain a synchronous mod-6 counter using J-K flipflops. **(10 Marks)**

8. Design a sequential machine using D-flipflops for realising the state table below. The machine is of a single input single output type.

Present state	Next state for input x=		Output Z for input x=	
	0	1	0	1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1

Indicate the state transition diagram. Does the state assignment. Work out the excitation and the output logics? **(20 Marks)**

** * **